AREA PLANNING & EFFECTIVE MGDI COMPLETE ACCESSORIES WITH POWERFUL TECHNOLOGY

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ABSTRACT

Full adders are utilized in many different appeals, in digital signal processors, microprocessors & microcontrollers, and are an essential component of the design of many digital systems. Great control is needed in electronic devices and circuits, which necessitates low power and rapid processing. The power gated MGDI complete full adder style analysis and design are displayed. Some low power complexity is retained in this entire adder. The presentation and appeal of MGDI full adder with existing adders, such as GDI and M-GDI. The solution of the power gated- MGDI full-adder demonstrated better power analysis values. Low power dissipation is decreased by using the MGDI Method while designing circuits. A MGDI approach enhances the threshold voltage drop and overcomes weak voltage swing output. Power gating is a method used in IC design to minimize power utilization by switching off the current to this circuit lumps, that are bared. The entire adder was constructed utilizing 45 nm technology and the Cadence tool's toggle drawing mode. It is based on the Power Gated- MGDI. The solution of power analysis obtained is 17.61uW & delay of 21.25e-9. It achieved 96.07%, 87.6%, 87.3%, 83.7% & 78.8% for Conventional full adder, 10T-GDI, 16T-Hybrid, 14T-MVT-GDI and 8T-M-GDI Technique. It achieved delay of 89.5%, 50%, 50.5%, 93% & 17.95% for Conventional full adder, 10T-GDI, 16T-Hybrid, 14T-MVT-GDI and 8T-M-GDI Technique. The construction of full adders for effective arithmetic operations and the installment of MASH and modulators for Sigma Delta DACs are two contemporary applications of the GDI technique that are also examined in this work.

1. INTRODUCTION

Nowadays, as the design complexities on IC chips are increasing exponentially. There is an urge to develop and examine such power reducing techniques which could provide low power consumption, less complex design, high speed performance and high reliability without compromising any functionality of a circuit design. Currently, the most popular technology used to design circuits is CMOS technology, but it dissipates a frequent power during transistor switching and also leakage current flow when not in switching activity (Zimmermann & Fichtner 1997, Morgenshtein 2010). Area systematic designs have demanded mathematical calculations at minimal power and fast-speed. Full adders are recognizable as a hallmark of great performance & low power. Full-adder architectures play

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a significant role in low power appeals (Solomon et al. 2018). In VLSI, some practices exist. They are nothing more than swiftly developing communication mechanisms and power. The VLSI design structure appears like its applications in that it has a high command. The full adder plays a predominant role in high-speed data communication architectonics in VLSI (Thamaraimanalan & Mohankumar 2022). A full adder is a useful implementation tool, just like network switches, digital signal processing, and processors. These characteristics contrasted with typical power, delay and speed. The current full adder circuits main goal is to minimized power dissipation and area. The GDI full adder, MGDI, and this power gated MGDI full adder are evaluated (Babu et al. 2022, Pearlin 2023, Kharade & Askhedkar 2023).

**Gate diffusion input**
A process for designing low-power digital combinatorial circuit especially in logic design called GDI. Digital circuit size, propagation-delay, and power utilisation can all be minimized while prolonging a low level of logic design complexity in the GDI method.

![Figure 1: Basic cell of GDI](image)

Even while the original GDI cell has many benefits, its performance degrades. In addition to this, typical p-well advancement does not allow for the physical installation of basic GDI cells. Furthermore, due to distinct wells for each transistor, would require the basic GDI cell has a larger area. This fundamental hypothesis is uncertain since the source and drain modules rely on input values. In present era, gate diffusion input is the single technique that is most popular. Two transistors are present in the Gate Diffusion Input (GDI) Method to create logic gates. Figure 1 describes GDI cell development. Although the GDI Formation is the same as an Inverter, It has Different Functionality 3 inputs are carried by GDI cell. As follows:
1. G serves as a gate-input of N-MOS & P-MOS transistors.
2. P serves as P-MOS transistor’s input.
3. N serves as the transistor's input.

The ability to create logic gates using two transistors is provided by GDI.

**Power gated MOD-GDI:**
By cutting off the current to circuit that are bared, power gating is utilized in IC design to minimize power usage. Power gating offers the advantage of enabling I\text{DDQ} testing in addition to lowering stand-by or leakage power. The following parameters are used in power gating techniques,

1. **Power gate size:**
   It must be chosen to accommodate switching current volume at any specific time. A larger gate is required so that there is no detectable voltage (IR) decrease as a result of the gate. The gate size is often chosen to be close to three times the switching capacitance. Additionally, designers have the option of using a P-MOS or N-MOS gate. Typically, N-MOS gates have a minimum surface area per unit of switching current. The switching current can be precisely measured using dynamic power analysis methods.

2. **Gate control slew rate:**
   In Power Gating, Power gating efficiency may be impacted since the slew rate is high, it takes longer to turn the circuit on and off. The gate control signal is buffered to adjust the slew rate.

**Modified gate diffusion input**

The fact being the exception is that the bulks of P-MOS & N-MOS transistors in M-GDI is consistently set to VDD & GND, it is quite alike to the basic GDI and fixes the problems that basic GDI cell had. As a result, the GDI gates can be easily realized in standard CMOS processes. The body's impact on circuit operation has a very similar outcome to that of a standard GDI cell.

MGDI has less power dissipation than CMOS logic architecture & GDI logic. CMOS innermost situations with regard to speed of the circuit, area of the total design, power-dissipation in the circuit, and power-delay, according to DC and Transient analysis carried out on more effective MGDI. This publication demonstrates low-voltage of the circuit, low power & minimum power-delay product are important, MGDI is the preferred logic design for realizing arbitrary combinational circuits.

![Figure 2: Basic MOD-GDI cell](image)
iii). Simultaneous switching capacitance:
This significant restriction is with the number of circuits that can be switched at once without endangering the integrity of the network. When a sizable section of the circuit is shift at once, the reported "rush current" risks integrity of the network. To avoid this, circuit must be changed gradually.

iv). Power gate leakage:
Leakage reduction is crucial as power gates are constructed from operating transistors, allowing for the greatest possible power savings.

Figure 3: Basic power gating

Figure 3 shows the fundamental power gated MOD GDI. Disconnecting the path to the power and ground terminals is one straightforward approach in such a circumstance. To accomplish this, a power gating circuit that can cut off the path when the circuit is dormant i.e., not in use.

when SLEEP = OFF (0)
- P-MOS & N-MOS sleep transistors on.
- The circuit runs in normal mode since P-MOS & N-MOS networks, linked to virtual VDD & GND, respectively.

when SLEEP = ON (1)
- PMOS and NMOS sleep transistors turn off.
- Because the direct channel from VDD to GND is cut off; leakage power is decreased.

2. LITERATURE SURVEY

The purpose of this research was to use GDI approach to construct a full adder with good performance. The design system clearly outperforms the other solutions presented as regards of area, delay, and power dissipation, according to make performance analysis table. Readings are accurate because the results were determined via simulation. In comparison to all existing procedures, this design will be faster and have a higher system efficiency. The design can be further altered by including a few extra transistors (Solomon et al. 2018).

This work describes the successful implementation of a low-power 8-bit GDI complete full-adder architecture using the variable body biasing technique in an EDA tool of 90nm. One of the low power techniques used in VLSI design, the VBB approach effectively lowers static power usage. A comparison of the solution in terms of power utilization and proportional delay was made using the complete adder circuit design in both traditional bias mode and VBB method mode (Kai, et al. 2019). It has been shown how modification of basic gates performed thorough performance examination. Tanner EDA and TSMC MOSIS a ±25nm technology were accelerated to verify and differentiate the performance of this M-GDI with traditional GDI and C-MOS logic as regards of transistor count, delay, and power dissipation. PTL performs poorly as regards of power consumption compared to M-GDI, GDI, and C-MOS because of lower output swings brought on by the threshold voltage drop over a single-channel transistor. Altogether, findings reveal that when compared to current GDI, C-MOS, and PTL, the updated primal and other topologies have the minimum delay, the lowest power consumption, and the fewest transistors (Uma & Dhavachelvan 2012). It was established that a different internal logic structure might be used to build full-adder cells. Two full-adders are constructed in conjunction as PTL powerless or groundless types of logic in order to illustrate its benefits. They were developed using TSMC's 0.18m C-MOS, and tested in simulations and contrasted with other recently announced energy-efficient full-adders (Aguirre-Hernandez & Linares-Aranda 2010, Radha 2020). The most effective strategy for adders provided in this study, in-between buffer insertion used during the modelling of the circuit topology, is discussed in an analysis to boost the direct power of adder cells (Aguirre-Hernandez & Linares-Aranda 2010).

In Section II of this study, the Gate Diffusion Input and Modified Gate Diffusion Input were methodically explained. Section III talks about the Modified Gate Diffusion with Power Gating Technique for Full Adder that is being proposed. Section IV discusses the outcomes of the Power Gated MGDI design. Section V presents a conclusion to the paper.

3. GDI & MGDI EXISTING TECHNIQUES

3.1 high speed adder using GDI technique
A full adder is crucial when developing a processor. The speed of operation becomes a critical consideration as the circuit complexity rises. There are several different
complete adder architectures available today. In this essay, we'll talk about how to use the Gate Diffusion Input approach to create a high-performance, low-power full adder. GDI is a specific modern approaches used to create logical circuits. This method will keep the complexity of the logic design minimal while reducing power-consumption in the circuit, propagation-delay of constructed circuit, and size of digital-circuits. This design performance is contrasted with the recent full adder designs of this high-speed adder.

GDI method is significantly more effective. Despite the technique's many benefits, there are a few issues that can be fixed. There are 3 inputs in a GDI cell. G serves as the input for both P-MOS & N-MOS, whereas P & N serves as input to source & drain. Hence the ability for construct a huge number of functions using the GDI approach is its main advantage. Table 2 shows that GDI may be used to implement a variety of designs, including MUX, AND, OR, and others. The design of a MUX, which can be accomplished with the use of two transistors, is the most difficult of them. While designing a MUX takes 8–10 transistors when using other traditional methods. Swing deterioration is the primary flaw with GDI method. This is caused by threshold loss, which must be eliminated using the very expensive.

### Table 1: Truth table for GDI-cell

<table>
<thead>
<tr>
<th>N</th>
<th>P</th>
<th>G</th>
<th>OUT</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>B</td>
<td>A</td>
<td>AB</td>
<td>F1</td>
</tr>
<tr>
<td>B</td>
<td>1</td>
<td>A</td>
<td>A+B</td>
<td>F2</td>
</tr>
<tr>
<td>1</td>
<td>B</td>
<td>A</td>
<td>A+B</td>
<td>OR</td>
</tr>
<tr>
<td>B</td>
<td>0</td>
<td>A</td>
<td>AB</td>
<td>AND</td>
</tr>
<tr>
<td>C</td>
<td>B</td>
<td>A</td>
<td>AB+AC</td>
<td>MUX</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>A</td>
<td>A</td>
<td>NOT</td>
</tr>
</tbody>
</table>

#### 3.2 Full adder using MGDI technique

Each high-speed digital system in the circuit, Digital Signal Processing system in the method, or control-system needs addition to function. Area, delay in the logical circuit, and power-dissipation are the main problems with adder cell design. Several devices need to be optimized for speed and power in low-voltage and low-power applications, which is a significant problem. Utilizing the Modified Gate Diffusion Input Technique can solve these problems. Through the use of this technology, digital circuit size, delay, and power consumption can be reduced, so logic design complexity is minimum. In this study, we emphasize two key design strategies. The performance difficulties of the former were contrasted with those of GDI and CMOS logic, and it presents the process of M-GDI.

The fundamental unit of the GDI-cell is a N-MOS & P-MOS with 4 terminals: G – represents common gate input of the N-MOS & P-MOS, P – denotes outer diffusion node of the P-MOS, N – denotes outer diffusion node of then N-MOS, & D – represents common diffusion node of P-MOS & N-MOS. This work implements modified-GDI in 0.250 m and compares them to existing GDI and C-MOS logic. A full-adder is a digital combinational logical circuit that produces the corresponding Sum, and Carry from the sum of 3 bits: A, B, and C. A, B, and C are 3 inputs to the full adder, and all of the test vectors have been produced and lead into the adder cell. At the time the inputs should reaches 50% of the supply voltage until last sum and carry reaching the required voltage level, cell delay gets detected. There is a total of eight input pattern combinations: 000, 001, 010, 011, 100, 101, 110, and 112. All transitions between these input combinations have been examined, and the latency for each transition has been determined.

### Table 2: Truth table for MGDI-full adder

<table>
<thead>
<tr>
<th>N</th>
<th>SN</th>
<th>P</th>
<th>SP</th>
<th>G</th>
<th>D</th>
<th>FUNCTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>A</td>
<td>A’</td>
<td>INVERTER</td>
</tr>
<tr>
<td>A</td>
<td>A</td>
<td>0</td>
<td>B</td>
<td>AB</td>
<td>AND</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>A</td>
<td>D</td>
<td>B</td>
<td>A+B</td>
<td>OR</td>
</tr>
<tr>
<td>A’</td>
<td>0</td>
<td>A</td>
<td>1</td>
<td>B</td>
<td>A’B+A’B’</td>
<td>XOR</td>
</tr>
<tr>
<td>A</td>
<td>0</td>
<td>A’</td>
<td>1</td>
<td>B</td>
<td>AB+A’B’</td>
<td>XNOR</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>B</td>
<td>B</td>
<td>A</td>
<td>A’B</td>
<td>FUNCTION 1</td>
</tr>
<tr>
<td>B</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>A</td>
<td>A’+B</td>
<td>FUNCTION 2</td>
</tr>
<tr>
<td>C</td>
<td>0</td>
<td>B</td>
<td>1</td>
<td>A</td>
<td>A’B+AC</td>
<td>MUX</td>
</tr>
</tbody>
</table>

**Figure 4:** Full adder using GDI-cell

**Figure 5:** Full adder using MGDI-cell
4. PROPOSED MGDI WITH POWER GATING FOR FULL ADDER

The power gated MGDI complete adder circuit design, which uses a modified process of GDI & M-GDI. The M-GDI full-adder has two expressions: Sum & Carry. Comparing the proposed/ constructed full adder circuit with GDI, and M-GDI full adders, it has lower power utilization and fewer-transistors in the logical circuits. The best method for low power applications & the speed of the power gated-MGDI design. This full adder's operation uses 3-inputs, which is simply A, B, and C_in, and 2-outputs namely Sum & Carry.

![Figure 6: Power Gated MGDI full adder](image)

Figure 6. shows the schematic figure for the Power Gating MGDI complete adder. P-MOS & N-MOS transistors, as well as ports like input pin, output pin, VDD and GND, are used to create the circuit in question. Compared to other methods, power gated M-GDI is unique. It is not produced strong 1 and a strong 0 as output step of the GDI approach. It is preferable to look for new customized ways to combat these GDI-cell drawbacks. Because of improper biasing at the bulk end, this circuit exhibits threshold drop. M-GDI is useful for creating high-speed, low-power circuits with less no. of transistors. Advantages of M-GDI design is to boosts the swing voltage output. It’s a allows top-down design. By cutting off the current to circuit that are bared, power gating is a technique used in IC design to minimize power-consumption. Power gating has the advantage of l_DDO testing to lowering stand-by or leakage power. When the GDI Complete Adder Circuit employs power gating technology, power is switched off when the circuit is lumped. In this instance, the circuit power dissipation can be minimized.

5. RESULT & DISCUSSION:

Powerful suggestion using the Cadence Virtuoso tool, Power gated modified gate diffusion input is built. It is made using advanced 45nm technology and can support up to 5 million system gates at the lowest possible cost.

A. Performance measure of gdi technique using full adder:
GDI Full-adder contains 3-inputs A, B, C_in and 2-outputs Sum & Carry. Finally, result is being prepared by applying Input Voltage of 1V, and the Transient response is given below in figure 7.

![Figure 7: GDI Output for Full Adder](image)

![Figure 8: M-GDI Output for Full Adder](image)

C. Performance measure of power gated mgdi technique using full adder:
Here, Power Gated MGDI Full-adder contains 3-inputs A, B, C_in and 2-outputs are Sum and Carry. Finally, result is being prepared by applying Input Voltage (VDC) of 1V, period of 20ns rise and fall time will be 1ps, pulse with is 10ns respectively. And the Transient response is given below in figure 9.

![Figure 9: Power Gated MGDI Output for Full Adder](image)
### Table 3: Comparison of Different Full Adders

<table>
<thead>
<tr>
<th>DIFFERENT FULL ADDER TECHNIQUES</th>
<th>POWER ANALYSIS (uW)</th>
<th>DELAY (e^9)</th>
<th>TRANSISTOR COUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional full adder (Weste &amp; Harris 2015)</td>
<td>448.3</td>
<td>203</td>
<td>28</td>
</tr>
<tr>
<td>10T-GDI (Lee et al. 2007)</td>
<td>142.5</td>
<td>42.50</td>
<td>10</td>
</tr>
<tr>
<td>16T-Hybrid (Bhattacharyya et al. 2014)</td>
<td>139.0</td>
<td>42.95</td>
<td>16</td>
</tr>
<tr>
<td>14T-MVT-GDI (Sanapala &amp; Sakthivel 2019)</td>
<td>107.8</td>
<td>309</td>
<td>14</td>
</tr>
<tr>
<td>8T-MGDI (Radha 2020)</td>
<td>83.2</td>
<td>25.9</td>
<td>8</td>
</tr>
<tr>
<td>Power gated MGDI (Proposed)</td>
<td>17.61</td>
<td>21.25</td>
<td>8</td>
</tr>
</tbody>
</table>

Above Figure 10 represent the comparison of Existing GDI and M-GDI Full Adders with the power analysis value of 448.3uW, 142.5 uW, 139.0uW, 107.8uW and 83.2uW & delay of 2.03e^-3, 42.50e^-9, 42.95e^-9, 3.009 e^-6 & 25.9e^-9, In proposed Power Gating MGDI full adder result achieved is 17.61 uW and 21.25e-9 respectively.

### Figure 10: Comparison of power Analysis & delay proposed vs Existing Full Adders

6. CONCLUSION

The implementation of several full adders utilizing GDI and M-GDI techniques are the main topics of this study. The table above represented a comparison of different full adders. Utilizing cadence tools, with schematic editor is L-editing in the toggle drawing mode, the simulation is accomplished. In this case of criteria, power analysis of this logical circuit & transistor count of power gated M-GDI full adder can be found. The output is good than the Conventional full adder, 10T-GDI adder, 16T-Hybrid adder, 14T-MVT-GDI adder and 8T-M-GDI full-adder. It achieved power analysis of 96.07%, 87.6%, 87.3%, 83.7% & 78.8% for Conventional full adder, 10T-GDI adder, 16T-Hybrid adder, 14T-MVT-GDI adder and 8T-M-GDI full-adder. It achieved delay of 89.5%, 50%, 50.5%, 93% & 17.95% for Conventional full adder, 10T-GDI, 16T-Hybrid, 14T-MVT-GDI and 8T-M-GDI Technique. It achieved delay of 89.5%, 50%, 50.5%, 93% & 17.95% for Conventional full adder, 10T-GDI, 16T-Hybrid, 14T-MVT-GDI and 8T-M-GDI Technique. Therefore, it is ideally suited for low power applications and the better power gated M-GDI full adder. Using these kinds of full adders in all multipliers and adders is the expansion and future focus of this paper.

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